Embedded Test for Highly Accurate Defect Localization

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***Abstract*—Modern diagnosis algorithms are able to identify the defective circuit structure directly from existing fail data without being limited to any specialized fault models. Such algorithms however require test patterns with a high defect coverage, posing a major challenge particularly for embedded testing.**
In mixed-mode embedded test, a large amount of pseudo-random (PR) patterns are applied prior to deterministic test pattern. Partial Pseudo-Exhaustive Testing (P-PET) replaces these pseudo-random patterns during embedded testing by partial pseudo-exhaustive patterns to test a large portion of a circuit fault-model independently. The overall defect coverage is optimized compared to random testing or deterministic tests using the stuck-at fault model while maintaining a comparable hardware overhead and the same test application time.
This work for the first time combines P-PET with a fault model independent diagnosis algorithm and shows that arbitrary defects can be diagnosed on average much more precisely than with standard embedded testing. The results are compared to random pattern testing and deterministic testing targeting stuck-at faults.

***Keywords*—BIST, Pseudo-Exhaustive Testing, Diagnosis, Debug**

I. Introduction

Latent defects are one of the main causes for reliability problems in semiconductors. These defects are characterized by the fact that they become critical and start to cause errors during the operation of the semiconductor in conjunction with aging, temperature differences or vibration. Many of these defects can be avoided by introducing changes in the design (such as re-sizing of transistors and interconnections). However, this requires the defect to be located first, which is impossible for test escapes and No-Trouble-Found-cases. With burn-in and corner-testing during volume test, a high cost is associated with finding these defects. Therefore, often an embedded test is used that tests the circuit structurally [1].

During embedded test, either random patterns, deterministic patterns or a combination of both (so called mixed-mode test) are used. The random patterns are generated by a linear feedback shift register (LFSR). Deterministic patterns are often generated using the stuck-at fault model and encoded in an appropriate manner [2–5]. The stuck-at fault model is widely used for its simplicity, but it models the behavior of latent production defects inadequately [6]. The defect coverage reachable by the stuck-at fault model can be enhanced by the N-detect approach [7] where each single stuck-at fault is tested at least N times (or as often as possible). The size of the required deterministic test set grows significantly for increasing values of N [8].

In order to not only detect, but also locate the potential defects, merely achieving a high defect coverage is not sufficient. In addition, the used test pattern set needs to provide detailed diagnosis information by provoking different test responses on the circuits outputs for all different defects.

The recently proposed partial pseudo-exhaustive test (P-PET) [9] replaces the random patterns in the first phase of mixed-mode testing with a pseudo-exhaustive test for a large part of the circuit. For an output x, $E_x = \{e_1, \ldots, e_n\}$ denotes the set of all inputs for which a structural path to x exists. The circuit structure between the inputs E_x and the output x is called a *cone*. A cone with output x is tested *pseudo-exhaustively* if all 2^{E_x} possible test patterns are applied to its inputs E_x.

In P-PET, instead of all circuit cones, cones up to a given size $|E_x| \leq \text{MAX}_{size}$ are tested pseudo-exhaustively. Multiple feedback polynomials of limited degree are calculated that control a programmable linear feedback shift register [10] in order to generate the exhaustive input assignments for the considered cones. As a result, the pseudo-exhaustive test pattern generation is applicable to the standard STUMPS architecture (Fig. 1). The required feedback polynomials are stored in the ROM (Fig. 1) to update the programmable LFSR during pattern generation. Hence, in comparison to PR testing, the hardware overhead of P-PET is negligible and consist of a few AND gates and a small ROM of a few hundred bits.

This approach is able to test on average 65% of the circuit structure of typical industrial designs pseudo-exhaustively with negligible hardware overhead, resulting in an significantly increased defect coverage compared to random patterns testing.

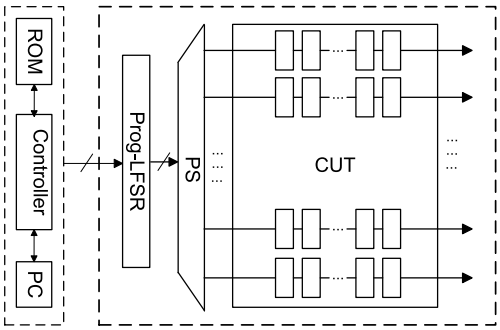

Fig. 1: Standard STUMPS Architecture.

Since the defect coverage is not a proper measure for the expected diagnostic resolution, this paper investigates for the first time the application of P-PET for optimizing the diagnosis of arbitrary defects.

The focus of the present work is the test pattern generation at the input side. Very efficient techniques are available for the extreme compaction of the circuit responses without compromising the diagnostic resolution [11, 12].

The rest of the paper is organized as follows. The next section presents the overview of underlying fault modeling approach called conditional line flip (CLF). In sections III and IV, we examine how P-PET patterns can increase the diagnostic resolution. Section V shows the effectiveness of diagnosis using P-PET patterns for industrial circuits.

II. Conditional Line Flip Calculus

We examine the diagnostic resolution for arbitrary defect using the Conditional Line Flip (CLF) calculus from [13]. A CLF consists of a victim signal and an arbitrary activation condition.

$$\text{Signal} \oplus [\text{Condition}]$$

The victim signal has an erroneous value if the condition is true. This condition can be arbitrarily selected, resulting in a CLF covering all possible defects that directly affect the specified victim signal. For example, an OR-bridge from signal a to signal b can be represented as a CLF as follows:

$$b \oplus [\overline{b} \wedge a].$$

The following analysis considers defects that affect only a single victim signal. This analysis can be easily generalized to larger defects by substituting every CLF with a tuple of CLFs.

III. Pseudo-perfect Diagnosability

Employing P-PET implies that all circuit cones up to a given size MAX_{size} are tested exhaustively. Figure 2 shows a circuit with two cones A and B which are tested exhaustively by the P-PET method. At the inputs of both A and B, all possible test patterns ($2^{|A|}$ and $2^{|B|}$) are applied.

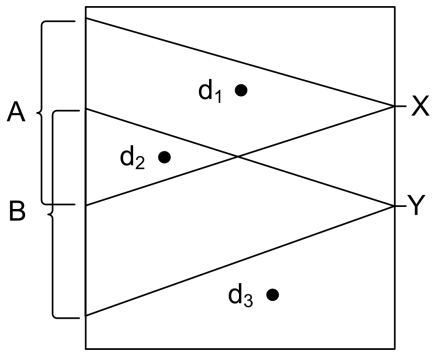

Fig. 2: Defects within and outside exhaustively tested cones.

Definition *Cone-local defect*: Let S_K be the set of all internal signals in a cone K. A defect $d = s \oplus [f(S_K)]$ with $s \in S_K$ and an arbitrary combinational function f over signal values is a cone-local defect in K.

In other words, a defect is cone-local in K, if both the victim signal as well as all the aggressor signals are included in K. In figure 2, d_1 is a cone-local defect in A, d_2 is cone-local in A and B, while defect d_3 is not cone-local in any of these cones. If a test pattern exists which makes a cone-local defect observable at the cone output, the P-PET test set will also cover this defect.

Definition *Pseudo-perfect Diagnosability*: A set of defects D with a given test set T and a given output o is pseudo-perfect diagnosable, if for every pair of defects $d_a, d_b \in D$ the following holds: If a test pattern exists which makes d_a and d_b distinguishable at the output o, the test set T also distinguishes these defects at this output.

The provocation of different responses is a necessary condition for distinguishing the defects by any diagnostic algorithm and the associated high diagnostic resolution. If a set of defects D with T at output o is pseudo-perfect diagnosable, no other test set exists that provides more diagnostic information at output o than T.

Theorem: Let K be a cone which is tested pseudo-exhaustively by the P-PET test set T. The set of all cone-local defects of a cone K

$$D_K = \{s_i \oplus [f(S_K)] | s_i \in S_K\}$$

is pseudo-perfectly diagnosable with T.

Proof: Without loss of generality, we choose a pair of defects $d_1, d_2 \in D_A$ (see figure 2). Suppose a test pattern exists that provokes different values at output X for these two defects. As the cone A is tested exhaustively, these defects will also generate different values for the P-PET pattern set. The same argument is true for two defects $d_1 = s \oplus [f(S_A)], d_1' = s \oplus [f'(S_A)] \in D_A$ that affect the same victim signal but have different conditions. By the exhaustive enumeration of cone A, all logically possible assignments of the signals in S_A are tested. Consequently, all assignments b are enumerated for f and f'. This especially includes all possible cones for which $f(b) \neq f'(b)$ holds. There is no other test set which provides more diagnostic information.

IV. Diagnostic Resolution of P-PET

A defect propagates usually to multiple outputs as most internal signals do. A defect could be observed at all these outputs, and therefore these outputs provide diagnostic information for this defect. Therefore, it needs to be investigated to what extent a defect is propagated to outputs that are pseudo-perfectly diagnosable by a P-PET pattern set.

Figure 3 shows a circuit with two outputs and 3 defects. The P-PET method only tests a portion of the circuit outputs pseudo-exhaustively. In figure 3 only output Y is tested exhaustively while output X is not tested exhaustively. Three propagation scenarios are possible now.

1) A defect propagates only to non-covered outputs (defect d_1 in figure 3).
2) A defect propagates to both covered and non-covered outputs (defect d_2 in figure 3).
3) A defect propagates only to covered outputs (defect d_3 in figure 3).

If a defect propagates to a covered output, it implies that the defect is situated in the corresponding cone. For instance, in figure 3, it is impossible for the defect d_1 to also propagate to the output Y.

The diagnostic resolution for a set of defects like d_1 is equivalent to that of a random test. The maximum diagnostic information can not be guaranteed at any output. For defects like d_2, the maximum diagnostic information is guaranteed for a subset of all possible observation points. Defects such as d_3 can be diagnosed perfectly as the maximum diagnostic information is guaranteed at all possible observation points.

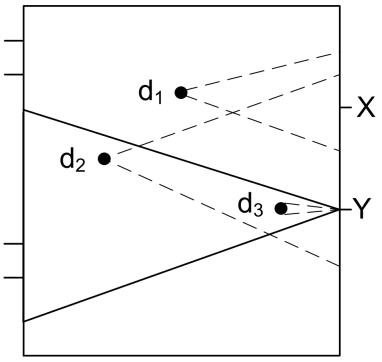

Fig. 3: Three propagation scenarios of defects.

A simple structural analysis can determine, which circuits portions can be perfectly diagnosed by a given P-PET pattern set.

V. Experimental Results

The P-PET approach is designed for large and flat industrial designs. The academic benchmark circuits (ISCAS85, ISCAS89) are too small [14] or have long paths which are very uncommon in real-world designs to show the effectiveness of P-PET. Therefore, the experiments were conducted on industrial circuits provided by NXP. For all the circuits, the P-PET scheme as presented in [9] is used to test the largest portion of the circuit pseudo-exhaustively. The results are reported in table I. The circuit name in the first column corresponds to the number of gates to the circuit. The next two columns present the number of pseudo-primary inputs and outputs. Column 4 shows the number of test patterns generated through the P-PET method, and the last column shows the proportion of the circuit which is tested pseudo-exhaustively as a percentage.

Circuit	#PPI	#PPO	#Patterns	%PE-tested
p35k	2912	2229	72544	33
p45k	3739	2550	16780955	49
p89k	4632	4557	25170456	26
p100k	5902	5829	33560334	44
p141k	11290	10502	50342938	29
p239k	18692	18495	58738945	55
p259k	18713	18495	50350359	60
p279k	18074	17827	100681365	47
p286k	18351	17835	100681642	37
p378k	15732	17420	134233460	79
p418k	30430	29809	83916506	43
p483k	33264	32610	92307947	47
p533k	33373	32610	134251094	45

TABLE I: P-PET Results.

Two sets of experiments were performed using these circuits. Firstly, a structural analysis was carried out to determine the diagnosability with P-PET test patterns. Secondly, comprehensive diagnostic experiments were carried out with a selection of all circuits.

A. Structural Analysis

By a simple traversing of the circuit structure, it was determined for each gate in the pseudo-exhaustively tested area whether the structural paths lead only to the covered outputs or in addition to non-covered outputs. The time complexity of this analysis is linear to the number of gates that belong to the P-PET covered part of the circuit. Table II displays these results.

Column 2 shows the proportion of a circuit for which all propagation paths end in covered outputs. The results show that the vast majority of circuit elements, which are pseudo-exhaustively tested, are also pseudo-perfectly diagnosable at all possible observation points. For small proportions of the circuits, not all the structural paths lead to exhaustively testable outputs (column %T), but the diagnosis result is still better than for random testing. The only exception is the circuit p378k, which has a very special structure and thereby is not comparable with the remaining circuits.

Circuit	% A	% T
p35k	31	2
p45k	41	8
p89k	21	5
p100k	37	7
p141k	26	3
p239k	51	4
p259k	57	3
p279k	43	4
p286k	34	3
p378k	14	65
p418k	36	7
p483k	41	6
p533k	41	4

TABLE II: A: Percentage of the gates, which are exclusively located in the exhaustively testable cones. T: Percentage of the gates, which are not exclusive, but are present in at least one exhaustively testable cone.

B. Diagnosis with P-PET

During this experiment, defects were randomly injected in selected circuits. The diagnosis algorithm from [15] was used to localize each injected fault. The defects were analyzed independently of each other with 3 different test pattern sets: A test pattern set generated by a commercial ATPG tool targeting stuck-at faults, a P-PET test pattern set, and a pseudo-random test pattern set of the same size as the P-PET pattern set.

The defect type of every diagnosed case was chosen randomly from standard bridging faults like wired-AND bridge, transition faults, stuck-at faults and cross-talk faults. The victim and the aggressor signals of the defects were randomly selected from the entire circuit, especially also from circuit parts that are not pseudo-exhaustively tested by the P-PET. This represents the worst-case, as in a real chip, bridges appear only between signals which are close to each other. The distance of signals in a layout corresponds to a certain degree to the structure of the logic circuit, as structurally associated circuit parts are placed close to each other in a layout. Real defects are therefore more often cone-local than in this experiment.

A diagnosis is treated as successful if one of the victim signals of the defect is returned as single best candidate. As soon as another candidate is reported to have the same probability, the defect is considered as not localized.

Table III shows the results of the diagnosis experiments. Column 2 shows the total number of defects considered one after each other. For each circuit and randomly selected defect, first a diagnosis with pseudo-random patterns was performed. These patterns were already able to isolate a majority of the defects perfectly. The number of defects that could not be located perfectly, is shown in column 3. For these cases, the diagnosis of the respective defect is performed with P-PET patterns and with ATPG patterns. Column 4 shows the number of additional defects which were perfectly diagnosed by P-PET patterns, while column 5 shows the number of defect perfectly diagnosed with ATPG patterns.

The results show that the diagnosis with P-PET test patterns is as successful as with ATPG patterns. In one case, the diagnosis success is in fact significantly higher. The diagnosis success of P-PET patterns corresponds very well to the results of the structural analysis in table II. There, among the five circuits, p45k showed the best P-PET coverage. If ATPG test patterns are used, the test access from the automatic test equipment (ATE) to the circuit under test (CUT) by using scan design for the needed bandwidth is a major cost factor, which can not be neglected. In contrast to testing with ATPG test patterns, the P-PET approach does not need any test data to be transferred to or stored on chip.

By generating the patterns on-the-fly on-chip a high bandwidth can be guaranteed while the overhead for storing the feedback polynomials is negligible. By just using a programmable feedback shift register and the corresponding polynomials, a significant increase in the diagnostic resolution of latent defects can be expected.

Circuit	Faults	PR-Pat. insufficient	(with P-PET-Pat. additional localized)	(with ATPG-Pat. additional localized)
p35k	2700	1559	53	76
p45k	2700	314	20	4
p89k	2700	583	20	17
p100k	900	72	4	1
p141k	325	56	4	4

TABLE III: Diagnosis success for arbitrary defects.

For circuit p35k an external test using ATPG patterns shows a higher defect coverage and diagnosability. As this circuit contains many small and some large cones, most of it's gates are not covered by P-PET. Table IV shows the used primitive polynomials together with the achieved circuit and gate coverage.

While 74% of all cones get covered by P-PET, the gate coverage is a low as 33%. This is also reflected by the highest degree of the used polynomials, which is 16. The associated low pattern count leads to the situation that all gates not being covered exhaustively (67%) are tested by relatively few random patterns.

Circuit	P-PET Test Set		Coverage (%)	
	Used Polynomials	#Patterns	Cones	Gates
p35k	$1 \times 2^{16} + 2 \times 2^{11}$	72544	74	33
p45k	1×2^{24}	16780955	57	49
p89k	$1 \times 2^{24} + 1 \times 2^{23}$	25170455	64	26
p100k	2×2^{24}	3356033	83	44
p141k	$2 \times 2^{24} + 2 \times 2^{23}$	50342935	45	29

TABLE IV: Used Primitive Polynomials and Achieved Circuit/Gate Coverage.

For the larger circuits P-PET employs at least one polynomial of degree 24. The resulting pattern set together with a significantly higher pattern count ensure a better random coverage for the not exhaustively tested and diagnosed circuit part. Together with the increasing number of small cones due to timing optimizations performed during circuit design and synthesis it can be concluded that the proposed embedded testing method is especially eligible for actual circuit sizes.

Cumulative effects such as multiple small delay faults along a speed path, that cause a certain output o to fail are also perfectly diagnosable by the approach described in the paper, if the input cone of o is covered by P-PET. If output o is covered in this way, all the off-path signals of the failing speed path are by definition within the cone and exercised exhaustively. However, although P-PET generates all logic value combinations within the cone, it does not generate all possible combinations of transitions which would be necessary for testing timing issues exhaustively. Experiments in this direction are certainly very interesting and we will consider the investigation of such timing issues in relation to P-PET for future work.

VI. Conclusion

This paper examines for the first time the application of P-PET testing for diagnosis of arbitrary defects using a fault-model-independent diagnosis algorithm. The structural analysis of typical industrial circuits shows, that most of the pseudo-exhaustively tested circuit parts are also pseudo-perfectly diagnosable at all possible outputs. The diagnosis experiments show that with P-PET pattern, significantly more defects can be perfectly diagnosed than with pseudo-random patterns. As compared to ATPG pattern P-PET shows a comparable diagnosis success, but convinces due to the omitted communication overhead and the lower hardware overhead for storing deterministic patterns.

VII. Acknowledgment

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