Michael E. Imhof

Publications

Awards

2014 **European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC)**, *Paper Award*.
[C26] GUARD: GUAranteed Reliability in Dynamically Reconfigurable Systems

2014 **IEEE European Test Symposium (ETS)**, *Best Paper Award*.
[C25] Variation-Aware Deterministic ATPG

2008 **IEEE International Symposium on Electronic Design, Test and Applications (DELTA)**, *Best Paper Award*.
[C3] Test Set Stripping Limiting the Maximum Number of Specified Bits

Journal Articles (refereed)

[J3] S. Holst, M. E. Imhof, and H.-J. Wunderlich, "High-Throughput Logic Timing Simulation on GPGPUs," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 20, no. 3, pp. 1–22, Jun. 2015. DOI: 10.1145/2714564.

[J2] L. Bauer, C. Braun, M. E. Imhof, M. A. Kochte, E. Schneider, H. Zhang, J. Henkel, and H.-J. Wunderlich, "Test Strategies for Reliable Runtime Reconfigurable Architectures," *IEEE Transactions on Computers*, vol. 62, no. 8, pp. 1494–1507, Aug. 2013. DOI: 10.1109/TC.2013.53.

[J1] R. Baranowski, S. Di Carlo, N. Hatami, M. E. Imhof, M. A. Kochte, P. Prinetto, H.-J. Wunderlich, and C. G. Zoellin, "Efficient Multi-level Fault Simulation of HW/SW Systems for Structural Faults," *SCIENCE CHINA Information Sciences*, vol. 54, no. 9, pp. 1784–1796, Sep. 2011. DOI: 10.1007/s11432-011-4366-9.

Conference Proceedings (refereed, formal proceedings)

[C27] A. Dalirsani, N. Hatami, M. E. Imhof, M. Eggenberger, G. Schley, M. Radetzki, and H.-J. Wunderlich, "On Covering Structural Defects in NoCs by Functional Tests," in *Proc. 23rd IEEE Asian Test Symposium (ATS)*, Hangzhou, China, Nov. 2014, pp. 87–92. DOI: 10.1109/ATS.2014.27.

[C26] H. Zhang, M. A. Kochte, M. E. Imhof, L. Bauer, H.-J. Wunderlich, and J. Henkel, "GUARD: GUAranteed Reliability in Dynamically Reconfigurable Systems," in *Proc. 51st ACM/EDAC/IEEE Design Automation Conference (DAC)*, HiPEAC Paper Award, San Francisco, CA, USA, Jun. 2014, pp. 1–6. DOI: 10.1145/2593069.2593146.

[C25] M. Sauer, I. Polian, M. E. Imhof, A. Mumtaz, E. Schneider, A. Czutro, H.-J. Wunderlich, and B. Becker, "Variation-Aware Deterministic ATPG," in *Proc. 19th IEEE European Test Symposium (ETS)*, Best Paper Award, Paderborn, Germany, May 2014, pp. 87–92. DOI: 10.1109/ETS.2014.6847806.

[C24] A. Dalirsani, M. E. Imhof, and H.-J. Wunderlich, "Structural Software-Based Self-Test of Network-on-Chip," in *Proc. 32nd IEEE VLSI Test Symposium (VTS)*, Napa, CA, USA, Apr. 2014, pp. 1–6. DOI: 10.1109/VTS.2014.6818754.

[C23] M. E. Imhof and H.-J. Wunderlich, "Bit-Flipping Scan - A Unified Architecture for Fault Tolerance and Offline Test," in *Proc. Design, Automation and Test in Europe (DATE)*, Dresden, Germany, Mar. 2014, pp. 1–6. DOI: 10.7873/DATE.2014.206.

[C22] R. Baranowski, A. Cook, M. E. Imhof, C. Liu, and H.-J. Wunderlich, "Synthesis of Workload Monitors for On-Line Stress Prediction," in *Proc. 16th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS)*, New York City, NY, USA, Oct. 2013, pp. 137–142. DOI: 10.1109/DFT.2013.6653596.

[C21] H. Zhang, L. Bauer, M. A. Kochte, E. Schneider, C. Braun, M. E. Imhof, H.-J. Wunderlich, and J. Henkel, "Module Diversification: Fault Tolerance and Aging Mitigation for Runtime Reconfigurable Architectures," in *Proc. IEEE International Test Conference (ITC)*, Anaheim, CA, USA, Sep. 2013, pp. 1–10. DOI: 10.1109/TEST.2013.6651926.

[C20] A. Czutro, M. E. Imhof, J. Jiang, A. Mumtaz, M. Sauer, B. Becker, I. Polian, and H.-J. Wunderlich, "Variation-Aware Fault Grading," in *Proc. 21st IEEE Asian Test Symposium (ATS)*, Niigata, Japan, Nov. 2012, pp. 344–349. DOI: 10.1109/ATS.2012.14.

[C19] M. S. Abdelfattah, L. Bauer, C. Braun, M. E. Imhof, M. A. Kochte, H. Zhang, J. Henkel, and H.-J. Wunderlich, "Transparent Structural Online Test for Reconfigurable Systems," in *Proc. 18th IEEE International On-Line Testing Symposium (IOLTS)*, Sitges, Spain, Jun. 2012, pp. 37–42. DOI: 10.1109/IOLTS.2012.6313838.

[C18] L. Bauer, C. Braun, M. E. Imhof, M. A. Kochte, H. Zhang, H.-J. Wunderlich, and J. Henkel, "OTERA: Online Test Strategies for Reliable Reconfigurable Architectures," in *Proc. NASA/ESA Conference on Adaptive Hardware and Systems (AHS)*, Nuremberg, Germany, Jun. 2012, pp. 38–45. DOI: 10.1109/AHS.2012.6268667.

[C17] D. A. Tran, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri, M. E. Imhof, and H.-J. Wunderlich, "A Pseudo-Dynamic Comparator for Error Detection in Fault Tolerant Architectures," in *Proc. 30th IEEE VLSI Test Symposium (VTS)*, Maui, HI, USA, Apr. 2012, pp. 50–55. DOI: 10.1109/VTS.2012.6231079.

[C16] A. Cook, S. Hellebrand, M. E. Imhof, A. Mumtaz, and H.-J. Wunderlich, "Built-in Self-Diagnosis Targeting Arbitrary Defects with Partial Pseudo-Exhaustive Test," in *Proc. 13th IEEE Latin-American Test Workshop (LATW)*, Quito, Ecuador, Apr. 2012, pp. 1–4. DOI: 10.1109/LATW.2012.6261229.

[C15] A. Mumtaz, M. E. Imhof, S. Holst, and H.-J. Wunderlich, "Embedded Test for Highly Accurate Defect Localization," in *Proc. 20th IEEE Asian Test Symposium (ATS)*, New Delhi, India, Nov. 2011, pp. 213–218. DOI: 10.1109/ATS.2011.60.

[C14] A. Mumtaz, M. E. Imhof, S. Holst, and H.-J. Wunderlich, "Eingebetteter Test zur hochgenauen Defekt-Lokalisierung," in *Proc. 5. GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf (ZuE)*, Hamburg-Harburg, Germany, Sep. 2011, pp. 43–47, ISBN: 978-3-8007-3357-6.

[C13] M. E. Imhof and H.-J. Wunderlich, "Korrektur transienter Fehler in eingebetteten Speicherelementen," in *Proc. 5. GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf (ZuE)*, Hamburg-Harburg, Germany, Sep. 2011, pp. 76–83, ISBN: 978-3-8007-3357-6.

[C12] A. Mumtaz, M. E. Imhof, and H.-J. Wunderlich, "P-PET: Partial Pseudo-Exhaustive Test for High Defect Coverage," in *Proc. IEEE International Test Conference (ITC)*, Anaheim, CA, USA, Sep. 2011, pp. 1–8. DOI: 10.1109/TEST.2011.6139130.

[C11] M. E. Imhof and H.-J. Wunderlich, "Soft Error Correction in Embedded Storage Elements," in *Proc. 17th IEEE International On-Line Testing Symposium (IOLTS)*, Athens, Greece, Jul. 2011, pp. 169–174. DOI: 10.1109/IOLTS.2011.5993832.

[C10] M. A. Kochte, C. G. Zoellin, R. Baranowski, M. E. Imhof, H.-J. Wunderlich, N. Hatami, S. Di Carlo, and P. Prinetto, "Efficient Simulation of Structural Faults for the Reliability Evaluation at System-Level," in *Proc. 19th IEEE Asian Test Symposium (ATS)*, Shanghai, China, Dec. 2010, pp. 3–8. DOI: 10.1109/ATS.2010.10.

[C9] M. A. Kochte, C. G. Zoellin, R. Baranowski, M. E. Imhof, H.-J. Wunderlich, N. Hatami, S. Di Carlo, and P. Prinetto, "System Reliability Evaluation Using Concurrent Multi-Level Simulation of Structural Faults," in *Proc. IEEE International Test Conference (ITC)*, Austin, TX, USA, Oct. 2010, p. 1. DOI: 10.1109/TEST.2010.5699309.

[C8] M. A. Kochte, C. G. Zoellin, R. Baranowski, M. E. Imhof, H.-J. Wunderlich, N. Hatami, S. Di Carlo, and P. Prinetto, "Effiziente Simulation von strukturellen Fehlern für die Zuverlässigkeitsanalyse auf Systemebene," in *Proc. 4. GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf (ZuE)*, Wildbad Kreuth, Germany, Sep. 2010, pp. 25–32, ISBN: 978-3-8007-3299-9.

[C7] M. A. Kochte, C. G. Zoellin, M. E. Imhof, R. Salimi Khaligh, M. Radetzki, H.-J. Wunderlich, S. Di Carlo, and P. Prinetto, "Test Exploration and Validation Using Transaction Level Models," in *Proc. Design, Automation and Test in Europe (DATE)*, Nice, France, Apr. 2009, pp. 1250–1253. DOI: 10.1109/DATE.2009.5090856.

[C6] M. E. Imhof, H.-J. Wunderlich, and C. G. Zoellin, "Erkennung von transienten Fehlern in Schaltungen mit reduzierter Verlustleistung," in *Proc. 2. GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf (ZuE)*, Ingolstadt, Germany, Sep. 2008, pp. 107–114, ISBN: 978-3-8007-3119-0.

[C5] M. E. Imhof, H.-J. Wunderlich, and C. G. Zoellin, "Integrating Scan Design and Soft Error Correction in Low-Power Applications," in *Proc. 14th IEEE International On-Line Testing Symposium (IOLTS)*, Rhodes, Greece, Jul. 2008, pp. 59–64. DOI: 10.1109/IOLTS.2008.31.

[C4] M. Elm, H.-J. Wunderlich, M. E. Imhof, C. G. Zoellin, J. Leenstra, and N. Maeding, "Scan chain clustering for test power reduction," in *Proc. 45th ACM/IEEE Design Automation Conference (DAC)*, Anaheim, CA, USA, Jun. 2008, pp. 828–833. DOI: 10.1145/1391469.1391680.

[C3] M. A. Kochte, C. G. Zoellin, M. E. Imhof, and H.-J. Wunderlich, "Test Set Stripping Limiting the Maximum Number of Specified Bits," in *Proc. 4th IEEE International Symposium on Electronic Design, Test and Applications (DELTA)*, Best Paper Award, Hong Kong, China, Jan. 2008, pp. 581–586. DOI: 10.1109/DELTA.2008.64.

[C2] M. E. Imhof, C. G. Zoellin, H.-J. Wunderlich, N. Maeding, and J. Leenstra, "Scan Test Planning for Power Reduction," in *Proc. 44th ACM/IEEE Design Automation Conference (DAC)*, San Diego, CA, USA, Jun. 2007, pp. 521–526. DOI: 10.1145/1278480.1278614.

[C1] M. E. Imhof, C. G. Zoellin, H.-J. Wunderlich, N. Maeding, and J. Leenstra, "Verlustleistungsoptimierende Testplanung zur Steigerung von Zuverlässigkeit und Ausbeute," in *Proc. 1. GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf (ZuD)*, Munich, Germany, Mar. 2007, pp. 69–76, ISBN: 978-3-8007-3023-0.

Workshop Contributions (refereed, non-formal proceedings)

[W4] A. Mumtaz, M. E. Imhof, and H.-J. Wunderlich, "Mixed-Mode-Mustererzeugung für hohe Defekterfassung beim Eingebetteten Test," in *Proc. 23rd GI/GMM/ITG Workshop Testmethoden und Zuverlässigkeit von Schaltungen und Systemen (TuZ)*, Passau, Germany, Feb. 2011, pp. 55–58.

[W3] M. A. Kochte, C. G. Zoellin, M. E. Imhof, R. Salimi Khaligh, M. Radetzki, H.-J. Wunderlich, S. Di Carlo, and P. Prinetto, "Modellierung der Testinfrastruktur auf der Transaktionsebene," in *Proc. 21st ITG/GI/GMM Workshop Testmethoden und Zuverlässigkeit von Schaltungen und Systemen (TuZ)*, Bremen, Germany, Feb. 2009, pp. 61–66.

[W2] M. E. Imhof, H.-J. Wunderlich, and C. G. Zoellin, "Integrating Scan Design and Soft Error Correction in Low-Power Applications," in *Proc. 1st Workshop on Low Power Design Impact on Test and Reliability (LPonTR)*, Verbania, Italy, May 2008, pp. 14–16.

[W1] M. E. Imhof, H.-J. Wunderlich, C. G. Zoellin, J. Leenstra, and N. Maeding, "Reduktion der Verlustleistung beim Selbsttest durch Verwendung testmengenspezifischer Information," in *Proc. 20th ITG/GI/GMM Workshop Testmethoden und Zuverlässigkeit von Schaltungen und Systemen (TuZ)*, Wien, Austria, Feb. 2008, pp. 137–141.